Silicon Photonic Carrier-Assisted Differential Detection Receiver With High Electrical Spectral Efficiency for Short-Reach Interconnects

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***Abstract*—Coherent detection is advantageous in achieving high electrical spectral efficiency (ESE) relative to direct detection (DD), due to its capability of field recovery. However, the stringent requirement on the laser sources prevents it from being widely utilized in cost-sensitive short-reach applications. Carrier-assisted differential detection (CADD) was proposed to retrieve the optical field without needing for a narrow-linewidth local oscillator (LO) in a receiver. To realize a compact CADD receiver, silicon photonic (SiP) integration is therefore of particular interest since it leverages the standard complementary metal-oxide semiconductor (CMOS) compatible fabrication, offering high yield, low cost, and compact footprint. The fabrication process does not introduce III-V materials as the CADD receiver is LO-free. In this article, we fabricated a SiP integrated CADD receiver and demonstrated the transmission and reception of a 240-Gb/s orthogonal frequency division multiplexing (OFDM) 16-ary quadrature amplitude modulation (16-QAM) signal transmitted over an 80-km single-mode fiber (SMF) link, with a bit error ratio (BER) below the 25% overhead (OH) soft-decision forward error correction (SD-FEC) threshold. To the best of our knowledge, we achieve a record 5.2-b/s/Hz ESE per polarization for an integrated DD receiver.**

***Index Terms*—Carrier-assisted differential detection, electrical spectral efficiency, short-reach interconnects, silicon photonic.**

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I. Introduction

THE development of the emerging applications, such as Internet of things, cloud computing, and high definition 8K video, has driven the continued exponential internet traffic growth in metropolitan and data center networks [1]. In these cost-sensitive short-reach applications, coherent detection is regarded as too costly due to the need for temperature-stabilized and narrow-linewidth laser sources [2], [3]. Hence, direct detection (DD) remains a preferred solution. Conventional intensity modulation and direct detection (IM/DD) scheme requires only one intensity modulator and one photodiode (PD), whereas the attainable reach is limited to few kilometers due to the power fading effect induced by the interplay between chromatic dispersion (CD) and square-law detection of the PD [4], [5], [6]. To extend the transmission distance, vestigial sideband (VSB) and single sideband (SSB) modulation are effective approaches which can overcome the CD limitation [7], [8], [9], [10], [11]. However, due to the nature of heterodyne detection, the electrical spectral efficiency (ESE) of the VSB/SSB scheme is intrinsically limited. Consequently, there has been growing interest in DD of complex-valued double sideband (DSB) signal analogous to the coherent detection which could be more electrical-spectral efficient. Although dual-SSB scheme was investigated for doubling the ESE of the signal, the optical bandpass filter (OBPF) with sharp roll-off is demanded for signal reception [12], [13], [14].

In [15], a promising carrier-assisted differential detection (CADD) scheme was proposed to retrieve the complex-valued DSB signal without employing optical filter or local oscillator (LO). Compared with conventional DD and self-coherent detection, although CADD potentially has a higher requirement on laser linewidth, the field recovery capability of complex-valued DSB signal contributes to a high capacity and ESE. Since the signal is recovered from the linear carrier-signal beating term in the CADD receiver, the achievable ESE approaches that of a single-polarization coherent homodyne detection receiver. In [16], the CADD experiment was conducted for the first time. The simplified CADD and generalized CADD receivers were investigated in [17], [18]. Aiming to pursue a higher ESE, a parallel dual delay-based CADD scheme was experimentally demonstrated in [19]. Compared with conventional DD and

coherent detection, CADD requires more components, such as an additional optical delay line and a PD. Thus, photonic integration of a CADD receiver is of particular interest since it effectively reduces the footprint and cost. CADD is a local oscillator (LO)-free scheme which does not introduce III-V materials in the standard complementary metal-oxide semiconductor (CMOS) manufacturing process. Therefore, the CADD receiver is well-positioned for silicon photonic (SiP) integration based on the CMOS platform with a high integration density and high yield [20], [21], [22], leading to a compact footprint and low cost.

Recently, we demonstrated a SiP CADD receiver for the first time in [23]. By employing SiP integration, the cost and footprint of the CADD receiver were reduced significantly. A 162-Gb/s net data rate and 4.6-b/s/Hz ESE per polarization was realized. In this paper, we further extend our work in [23] as follows: (i) we elaborate the motivation of our work by comparing CADD receiver with conventional DD and coherent detection receivers; (ii) we provide the detailed design and fabrication of the SiP CADD chip; (iii) we achieve a higher capacity and ESE by reducing the frequency gaps between neighboring sub-band signals. In the experiment, 240-Gb/s (net 182-Gb/s) orthogonal frequency division multiplexing (OFDM) 16-ary quadrature amplitude modulation (16-QAM) signal is successfully detected and recovered with the SiP CADD receiver after transmitted over an 80-km single-mode fiber (SMF) link. The bit error ratio (BER) is below the 25% overhead (OH) soft-decision forward error correction (SD-FEC) threshold of 5×10^{-2}. To the best of our knowledge, we achieve a record ESE per polarization of 5.2 b/s/Hz for an integrated DD receiver.

The rest of this paper is organized as follows. In Section II, we compare the conventional DD, coherent detection, and CADD schemes. Section III illustrates the design and fabrication results of the SiP CADD chip. In Section IV, we describe the experimental setup and digital signal processing (DSP) algorithms. Section V presents the experimental results and discussion. Finally, we draw the conclusions in Section VI.

II. Comparison of Different Detection Schemes

The structures of the conventional DD and coherent detection receivers are shown in Fig. 1(a) and (b), respectively. Conventional DD relies on only one PD for signal reception, thus has the merit of simple implementation and low cost. However, the phase information is lost due to the square-law detection of the PD, limiting the achievable capacity and ESE. On the other hand, a coherent receiver consists of a LO, a 90-degree optical hybrid, and two balanced PDs (BPDs). Through the linear beating between the received signal and the carrier from the LO, coherent detection is capable of retrieving both the intensity and phase information. Therefore, a complex-valued DSB signal with high ESE can be transmitted and recovered. Moreover, benefiting from the access to the optical field, the transmission impairments and distortions including CD can be compensated, enabling a superior performance. However, the utilization of low-linewidth LO not only increases the cost, but also introduces frequency offset and carrier phase issues. As a result, for cost-sensitive short-reach interconnects, a DD scheme capable of recovering a complex-valued DSB signal is highly desired to lower the cost and DSP complexity.

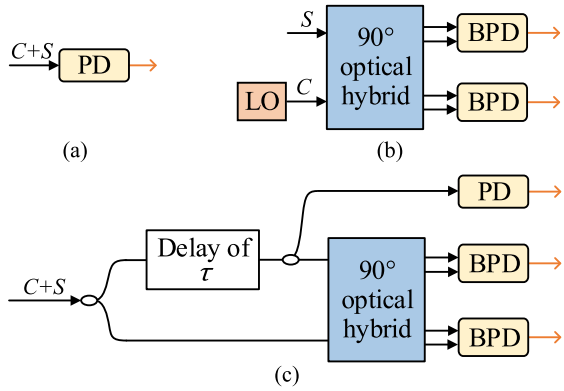

Fig. 1. Structures of (a) the conventional DD receiver, (b) the coherent detection receiver, and (c) the CADD receiver.

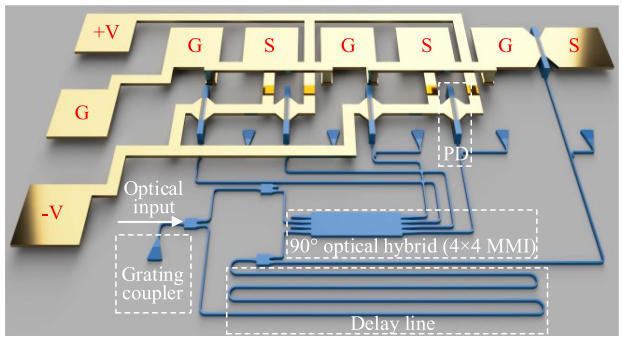

Fig. 2. 3-D illustration of the designed SiP CADD receiver.

Fig. 1(c) illustrates the architecture of the CADD receiver, which is composed of two optical couplers, an optical delay line, a 90-degree optical hybrid, and five PDs [15]. Without needing for a LO, CADD can realize optical field recovery as coherent detection does. Therefore, CADD has the combined merits of conventional DD and coherent detection, thus attracting increased interests [15], [16], [17], [18], [19]. As indicated in Fig. 1, more components are required in the CADD receiver, i.e., an optical delay line and a PD. To reduce the cost and footprint, photonic integration can be adopted. The LO-free feature of the CADD receiver eliminates the need for III-V materials. Therefore, CMOS-compatible SiP integration technology becomes a promising solution featuring high yield and low cost [20], [21], [22]. Although the cost of the coherent receiver can be reduced using integration, it is still considered costly due to the employment of the LO, which requires heterogeneous integration of III-V material. Moreover, the precise wavelength alignment between transceiver lasers and the temperature control of the narrow-linewidth LO lead to a high cost and power consumption.

III. Silicon Photonic CADD Receiver Chip

Fig. 2 depicts the three-dimensional (3-D) illustration of the designed SiP CADD receiver chip. Grating coupler is utilized

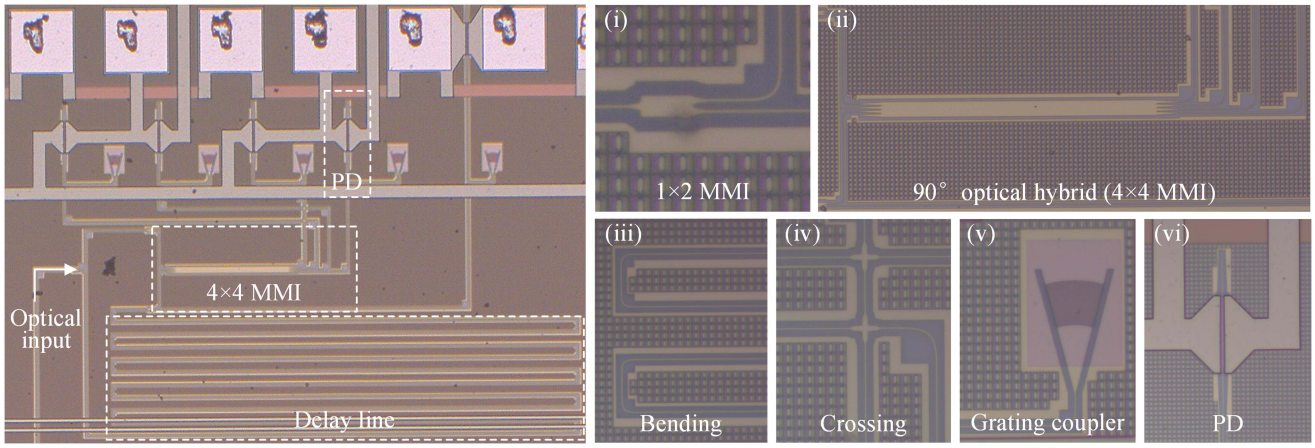

Fig. 3. Microscope image of the SiP CADD receiver. Insets (i-vi): magnified micrographs of the 1 × 2 MMI, 4 × 4 MMI, bending, crossing, grating coupler, and PD, respectively.

to launch the signal to the silicon chip. A 1 × 2 multimode interferometer (MMI) functions as a 50:50 coupler to split the incident light into two branches, one of which undergoes a delay line to obtain the delayed signal. For the CADD receiver, the optical delay, carrier-to-signal power ratio (CSPR), and guard band need to be jointly optimized. In this work, we firstly set the optical delay based on the transceiver's bandwidth constraint, then optimize the CSPR and guard band in the experiment. Considering the bandwidth limitation of the devices including the high-speed probes and cables, the delay value is selected as 111 ps in this work, corresponding to a waveguide length of 7750 μm. The delay can be optimized in the future work. The signal together with one of the delayed paths are input to the 90-degree optical hybrid. Here, we design a 4 × 4 MMI to provide a 90-degree optical hybrid function. After the differential detection, the outputs of the 4 × 4 MMI are fed into four single-ended PDs, which are combined to function as two BPDs. Additionally, the other branch of the delayed signal is detected with another single-ended PD. Finally, three photocurrents are read out with high-speed probes and cables, and captured using a digital scope.

We fabricated the devices on a 220-nm commercial silicon-on-insulator (SOI) wafer with standard CMOS manufacturing process. Fig. 3 shows the microscope image of the SiP integrated CADD receiver, with a size of about 1.1 mm × 0.9 mm. On-chip components are connected using the 450-nm width silicon waveguides with an insertion loss (IL) of less than 1.5 dB/cm. Insets (i-vi) illustrate the magnified micrographs of the 1 × 2 MMI, 4 × 4 MMI (10 μm × 180 μm), bending, crossing, grating coupler, and PD, respectively. With 0-V and 3-V reverse bias voltages, the on-chip germanium PD has a reported 3-dB bandwidth of 21 GHz and 33 GHz, respectively. The reverse bias voltage was set to 3V in the experiment for a high-speed transmission demonstration. The period of the Al pads is 150 μm, and each pad occupies an area of 100 μm × 100 μm to facilitate the pad-probe contact. Table I lists the typical performance of the components utilized on the chip. Note that the aim of this work is to demonstrate a high-ESE SiP DD receiver based on the CADD scheme proposed in [15] which is well-positioned for integration. The optimization of the fabricated receiver may be studied in future work.

TABLE I
TYPICAL PERFORMANCE OF THE DEVICES EMPLOYED ON SIP CADD CHIP

Devices	Performance at 1550 nm	
1×2 MMI	IL < 0.3 dB	Imb < 0.5 dB
4×4 MMI	PE < 5°	Imb < 1 dB
Bending	IL < 0.017dB/90°	
Crossing	IL < 0.1 dB	
Grating coupler	IL < 4.0 dB/facet	
PD	Res_{-1V} > 0.9 A/W	DC_{-1V} > 80 nA

PE: Phase Error, Imb: Imbalance, Res: Responsivity, DC: Dark current.

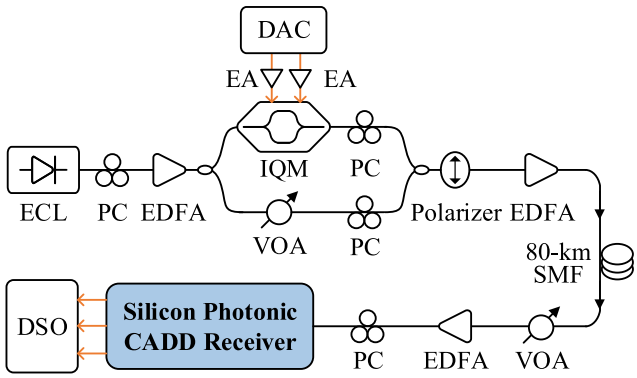

Fig. 4. Experimental setup. ECL: external cavity laser. PC: polarization controller. EDFA: erbium-doped fiber amplifier. DAC: digital-to-analog converter. EA: electrical amplifier. IQM: IQ modulator. VOA: variable optical attenuator. SMF: single-mode fiber. DSO: digital storage oscilloscope.

IV. EXPERIMENTAL SETUP AND DSP ALGORITHMS

Fig. 4 presents the experimental setup for SiP CADD-based 240-Gb/s transmission. Since CADD is free of LO and sharp-roll-off optical filter, it is expected to have a good tolerance to laser linewidth and wavelength stabilization, which allows

Binary data
OFDM mapping
IFFT
Resampling
Pre-emphasis
Clipping

(a)

Resampling
Synchronization
FFT
Equalization
SSBI cancell.
BER

(b)

Fig. 5. DSP algorithms in the transmitter (a), and receiver (b), respectively.

for using uncooled distributed feedback (DFB) lasers. In this proof-of-concept experiment to characterize the performance of the silicon chip, we employ an external cavity laser (ECL) with a 15-kHz-linewidth to output a 10-dBm light, which is amplified by an erbium-doped fiber amplifier (EDFA) and then split into two paths: one for the electrical-to-optical (E/O) modulation and the other serves as the optical carrier. The input optical power to the IQ modulator (IQM) is 15.5 dBm. A digital-to-analog converter (DAC) (Micram DAC4) operating at a sampling rate of 100 GSa/s generates the 240-Gb/s OFDM 16-QAM signal. The amplified signal after the electrical amplifiers (EAs) drives a 35-GHz IQM which is biased at its transmission null. Then, the carrier-suppressed modulated signal and the optical carrier form a complex-valued DSB signal. Two polarization controllers (PCs) and a polarizer are utilized to align the polarization states between the signal and the carrier along the axis of the polarizer. We optimize the carrier-to-signal power ratio (CSPR) by tuning the variable optical attenuator (VOA) placed at the carrier path. In the optical back-to-back (OBTB) case, the carrier-assisted signal output by the polarizer is input to the receiver-side VOA, while the signal is amplified with an EDFA and launched into an 80-km SMF link in the transmission case. At the receiver side, another VOA is employed for varying the received optical power (ROP), followed by an EDFA to compensate the fiber link loss. Before entering the SiP CADD receiver, the polarization state of the signal is aligned with the silicon chip using a PC. Finally, the outputs from the chip are read out with high-speed probes and collected by an 80-GSa/s digital storage oscilloscope (DSO) (LeCroy 36Zi-A).

The transceiver DSP algorithms are given in Fig. 5. In the transmitter, the binary data is mapped to 16-QAM symbols. For the generation of the OFDM signal, a 4096-size fast *Fourier* transform (FFT) is used, with 3072 subcarriers filled with 16-QAM symbols. Then, interleaved training sequence, in which only the odd subcarriers are filled with symbols, is added before the payload for channel response estimation. To deal with the imperfect frequency response of the transmitter, frequency-domain pre-emphasis is implemented. Before the signal is loaded to the DAC, the peak-to-average-power ratio (PAPR) is clipped and optimized. In the receiver, the captured signals are resampled to a sampling rate of 160 GSa/s. After frame synchronization, the signals are reconstructed according to the principle of CADD, followed by channel equalization and iterative SSBI cancellation. Finally, the BER is calculated by error counting of $\sim 1 \times 10^6$ bits to evaluate the performance.

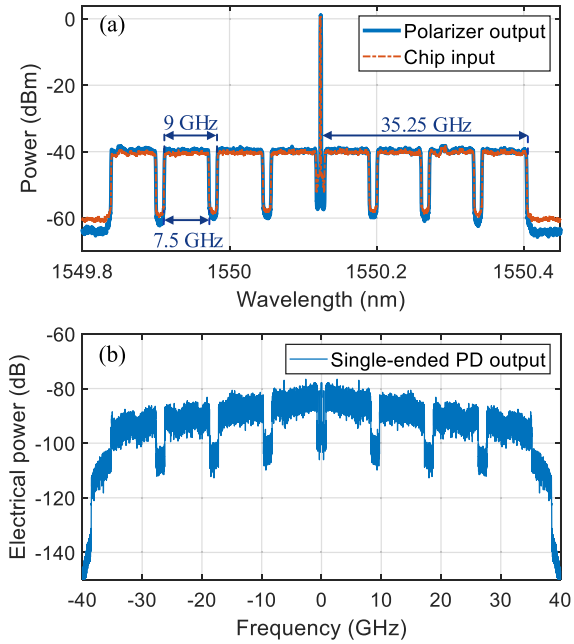

Fig. 6. (a) Optical spectra at different stages in the transmission case. (b) Electrical spectrum of the signal monitored by single-ended PD in the SiP CADD receiver.

V. Experimental Results and Discussion

Fig. 6(a) plots the optical spectra of the signals at different stages in the transmission case, with a resolution of 1.12 pm. The CADD receiver features a transfer function originated from the delay line and the optical hybrid [15]. When the magnitude of the transfer function is less than 1, the SSBI is amplified. Therefore, to prevent the signal from suffering enhanced SSBI distortion, the guard band is essential in certain frequency regions, especially around the transmission nulls of the transfer function where the SSBI is severely amplified. As indicated in Fig. 6(a), an 8-band loaded OFDM 16-QAM signal is designed in the experiment, with each sub-band occupying 7.5 GHz, corresponding to a data rate of 240 Gb/s. There is a 1.5-GHz guard band inserted between two neighboring sub-bands, resulting in an electrical bandwidth of 35.25 GHz. To realize a higher capacity and ESE, the spectrum overhead is reduced compared with that in [23]. The guard band is a trade-off between the ESE and BER performance. It can be observed that the high-frequency attenuation is mitigated with pre-emphasis in the transmitter DSP. Fig. 6(b) shows the electrical spectrum of the signal detected by single-ended PD in the SiP CADD receiver. Since transmitter-side bandwidth limitation is addressed with pre-emphasis, the roll-off of the spectrum is caused by the bandwidth constraint of the receiver, which mainly comes from the on-chip PD, the high-speed probe, the cable, and the DSO.

We first determine the PAPR of the generated OFDM signal by optimizing the BER performance. The signal with a high PAPR normally suffers from severe DAC quantization noise, and the receiver sensitivity could be degraded. As shown in Fig. 7(a), the optimal PAPR values for two cases are both 10 dB. In addition to PAPR, we investigate the impact of CSPR on the

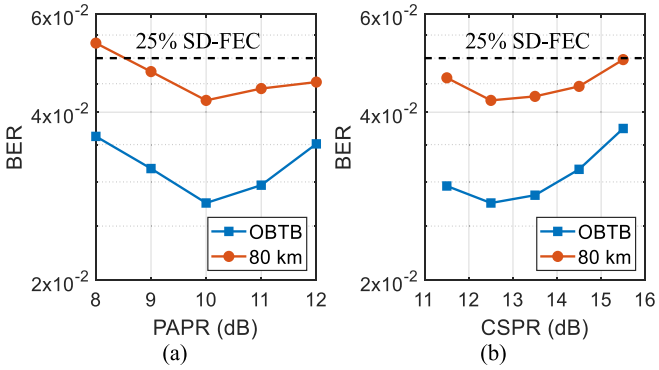

Fig. 7. (a) BER versus PAPR in the OBTB case and after the 80-km fiber transmission. (b) BER versus CSPR in two cases.

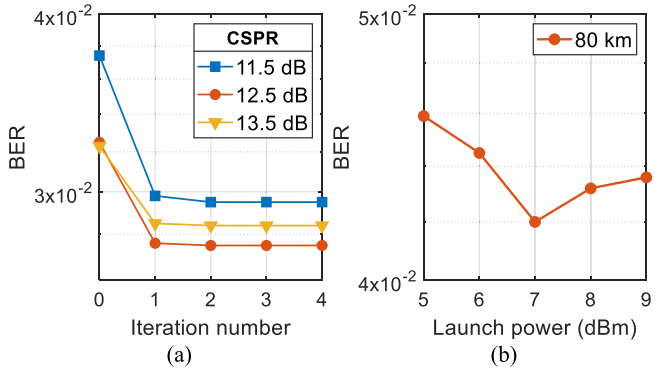

Fig. 8. (a) BER as a function of iteration number of the SSBI cancellation algorithm under different CSPR value conditions. (b) Optimization of the launch power.

BER performance. Since the desired linear term is contaminated by the SSBI, a high CSPR helps to mitigate the effect of the SSBI distortion. Nevertheless, this reduces the effective signal power since the carrier bears no information, thus the receiver sensitivity is sacrificed. Hence, the CSPR is optimized both in the OBTB and transmission cases. To calculate the CSPR, we measure the power of the signal and carrier after the PCs in each path, respectively. Through adjusting the VOA in the carrier branch, the CSPR value is varied. As shown in Fig. 7(b), the optimum CSPR is 12.5 dB for both cases. Note that since we aim to achieve a high capacity and ESE in this work, a narrow frequency gap is designed between two sub-bands. Consequently, part of the signal components occupies the SSBI-enhanced frequency region, resulting in a high optimal CSPR value for SSBI mitigation. To relax the CSPR requirement, we can insert a larger guard band or research on more effective SSBI cancellation techniques.

Fig. 8(a) plots the BER as a function of iteration number of SSBI cancellation algorithm under different CSPR value conditions in the OBTB case. The first iteration brings significant BER reduction, manifesting the effectiveness of the deployed iterative algorithm. Due to the high CSPR in the experiment, the BER performance gets saturated after two iterations. Fig. 8(b) illustrates the optimization of the launch power in the transmission case. The lowest BER is realized with a 7-dBm launch power.

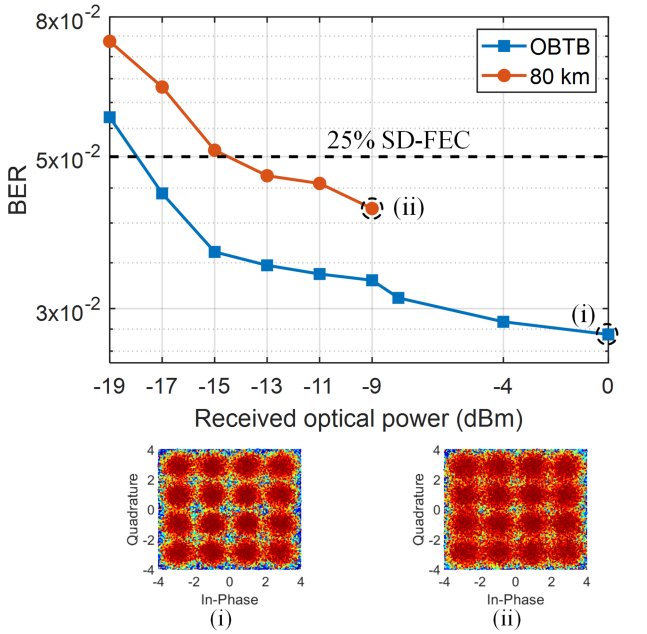

Fig. 9. BER versus ROP in the OBTB case and after the 80-km transmission. Insets (i-ii) constellations in the OBTB case at 0-dBm ROP and after the fiber transmission at –9-dBm ROP, respectively.

Fig. 9 shows the BER versus ROP in the OBTB and transmission cases, with the insets (i-ii) showing the constellations in the OBTB case at 0-dBm ROP and after the fiber transmission at –9-dBm ROP, respectively. After the 80-km SMF transmission, 240-Gb/s OFDM 16-QAM signal is successfully recovered with the BER below the 25% OH SD-FEC threshold of 5×10^{-2} [24], [25]. Compared with the work in [23], since the guard band was reduced and more signal components occupy the SSBI-enhanced region, the BER was higher and thus 25% FEC threshold of 5e-2 BER [24], [25] was introduced. We aim to achieve a high capacity and ESE with SiP CADD in this work, thus the results of lower rates were not demonstrated. The required receiver bandwidth is 35.25 GHz, thus achieving a 5.2-b/s/Hz ESE. As aforementioned, part of the enhanced SSBI distortions is overlapped with the information-bearing signals. Besides, it can be observed from Fig. 6(b) that the detected signal suffers from severe bandwidth limitation. Moreover, some fabrication differences may exist between the two PDs which are combined to realize a BPD, resulting in nonzero and slightly different responsivity. All these reasons lead to a relatively high BER in this work. To further improve the performance of the CADD receiver, we can optimize the transfer function of the receiver to suppress the SSBI-amplified frequency regions, or introduce better SSBI cancellation schemes to mitigate the SSBI distortions. Besides, the orthogonalization algorithms to compensate O-E front-end imbalance are expected to lower the BER. The transmission sensitivity penalty is mainly attributed to severer analog-to-digital converter (ADC) quantization noise caused by the increased PAPR, and the noise is amplified after implementing the transfer function. Moreover, the transmitter-side EDFA introduces excess amplified spontaneous emission (ASE) noise.

TABLE II
EXPERIMENTAL DEMONSTRATIONS BASED ON INTEGRATED DD RECEIVERS

Receiver structure	Modulation format	Raw/Net data rata (Gb/s)	Distance (km)	Field recovery capability	# of needed polarizations	Net data rata per polarization (Gb/s)	Required receiver bandwidth (GHz)	ESE per polarization (b/s/Hz)
SiP PD [26]	SSB OFDM 16-QAM	112/93	80	Y	1	93	28	3.3
SiP SV-DD [27]	DSB 16-QAM	240/224	40	Y	2	112	33	3.4
SiP PD [28]	DSB PAM4	200/187	1.5	N	1	187	50.5	3.7
SiP SV-DD [29]	DSB 16-QAM	128/119	100	Y	2	59.5	16	3.7
SiP PD [30]	DSB PAM4	106/100	0	N	1	100	26.5	3.8
SiP BPD [31]	DSB adaptively-loaded OFDM	140/131	2	N	1	131	33.8	3.9
SiP CADD [23]	DSB OFDM 16-QAM	224/162	80	Y	1	162	35	4.6
SiP BPD [31]	DSB adaptively-loaded OFDM	173/162	0	N	1	162	33.8	4.8
SiP CADD (this work)	DSB OFDM 16-QAM	240/182	80	Y	1	182	35.25	5.2

Table II provides the comparison of state-of-art work based on integrated DD receivers. For conventional IM/DD systems, the transmission distance and ESE are both limited due to the lack of field recovery capability [28], [30]. To achieve a high ESE, adaptively loading with up to 128-QAM was employed in [31]. However, leveraging higher-order modulation format imposes a more stringent requirement on the effective number of bits (ENOBs) of the ADC and DAC, and the received signal-to-noise ratio (SNR). By transmitting the SSB signal, the attainable reach can be increased, while the heterodyne detection nature restricts the ESE [26]. Although the SV-DD is capable of field recovery of complex-valued DSB signal, the carrier, and the modulated DSB signal respectrively occupy the two orthogonal polarizations in the SiP SV-DD demonstrations [27], [29], which sacrifices the ESE on per polarization basis. On the other hand, CADD is able to recover the carrier-assisted complex-valued signal using only one polarization. As evidenced by the table, we achieve the highest 5.2-b/s/Hz ESE per polarization for an integrated SiP DD receiver. To achieve even higher capacity and ESE, polarization multiplexing transmission with two single-polarization CADD receivers could be utilized, where an edge coupler, a dynamic polarization rotator, and a polarization beam splitter are required to split the dual-polarization signal for detection.

VI. CONCLUSION.

In conclusion, we demonstrated a 240-Gb/s complex-valued DSB OFDM 16-QAM signal transmitted over an 80-km SMF link based on a SiP CADD receiver. We achieved a 182-Gb/s net data rate with a 5.2-b/s/Hz ESE. To our best knowledge, a record ESE per polarization for an integrated DD receiver is realized. CADD has the capability of recovering the optical field without using LO, at the expense of more components including an optical delay line and a PD. By leveraging the CMOS-compatiable SiP integration technique, the large component count issue of the CADD receiver is well-addressed, contributing to a compact footprint and a reduced implementation cost. Hence, we believe that our LO-free and CMOS-compatible SiP CADD receiver provides promising potential in cost-effective passive optical networks (PONs), mobile fronthaul systems, and short-reach interconnects.

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