Sampling-phase optimised duobinary receiver enabling improved dispersion tolerance

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A novel optical duobinary detection scheme that optimises the sampling phase of the receiver based on preliminary sequence decision is proposed. Simulation results show significant improvement in dispersion tolerance and back-to-back sensitivity. An implementation using an over-sampling frontend, which is compatible with other designs of electrical dispersion compensation receivers, is also proposed.

Introduction: Partial-response modulation [1–4], such as duobinary signalling, and electrical dispersion compensation (EDC) techniques [5–7], have become viable solutions to mitigate the effects of chromatic dispersion (CD). Their combination could further extend transmission distance without use of dispersion compensating fibre (DCF) [8, 9]. Improving back-to-back (BB) sensitivity and the dispersion tolerance of duobinary systems have been the focus of recent studies. An over-sampling duobinary receiver can significantly improve BB sensitivity, but not dispersion tolerance [10].

In this Letter, we propose a relatively simple, yet effective, duobinary receiver design based on sequence-decision assisted sampling-phase optimisation (SASO). It can effectively reduce the deterministic timing jitter induced by the inter-symbol interference (ISI). It leverages the knowledge of the data sequence estimation to implement the bit-by-bit sampling phase adaptation, which fundamentally distinguishes it from the previous oversampling receivers [10].
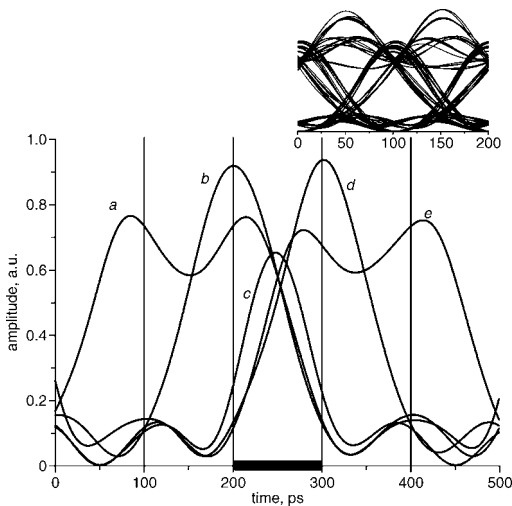

Fig. 1 *Dispersion-induced duobinary signal 'jitters' after transmission over 200 km of SSMF*

Data patterns associated with the different waveforms are: *a* 11100; *b* 01100; *c* 00100; *d* 00110; *e* 00111
Inset: Simulated eye diagram

Dispersion-induced deterministic timing jitter: Simulated 10 Gbit/s duobinary waveforms (Fig. 1) illustrate the relationship between the data patterns and timing jitter of duobinary signals under large residual dispersion conditions. A lowpass filter-based duobinary transmitter is employed in the simulation [4], and a $2^{10} - 1$-long pseudorandom bit sequence is used. The average launch power is 3 dBm, which is typical in short-haul links [4]. Transmission over spans of 80 km standard singlemode fibre (SSMF) without DCF is simulated.

Our receiver model consists of an ideal *pin*, a fifth-order 7 GHz bandwidth Bessel filter, a sampling circuitry with finite timing accuracies [7], and the digital signal processing logic that implements our proposed detection algorithm (when applicable). The Monte Carlo method is used to calculate the required optical signal-to-noise ratio (OSNR) to achieve a certain bit error rate (BER), e.g. BER = 10^{-3}, the FEC threshold of the enhanced FEC [4].

In Fig. 1, the eye diagram is closed as the edges of the bits, under certain cases, shift inwards towards the centre of the bit period, even though the peak powers of the 'one' bits remain large. This bit-by-bit

timing 'jitter' is determined by the transmitted data pattern; within the range of 200 km of SSMF, it is determined by the patterns of any five consecutive bits (see Fig. 1).

Proposed SASO scheme: Our idea to combat this 'jitter' is to adjust the sampling phase dynamically so that it follows the shifts of the edges of the bit. Since accurate sampling timing adjustment at such a high speed is impossible to implement with current technologies, we propose instead a design comprising an over-sampling frontend, a bank of conventional hard-decision gates in parallel, and a digital processing unit.

As in Fig. 2, the frontend samples the received waveform of each bit at N ($N = 3$, here) consecutive timing positions that are separated by a time shift Δ from each other. Δ is adjusted based on the amount of ISI jitter; in our case it is set to 0 ps within the first 100 km of transmission and gradually increased up to 20 ps for a distance of 250 km. The decision gates yield preliminary hard decision results from each corresponding sampled output. For simplicity, the decision threshold is the same for the three gates but optimised for different amounts of dispersion. Note that the frontend and decision gates can be readily realised with sufficient phase adjustment accuracy [7].
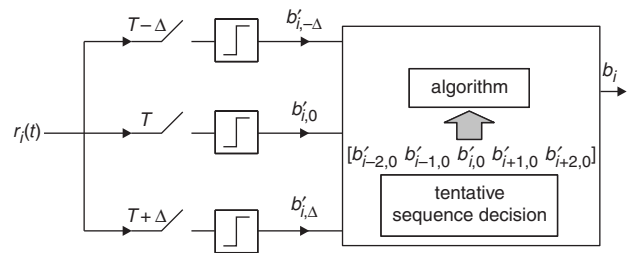

Fig. 2 *Schematic of SASO receiver*

The following digital circuitry generates the final decision of the current bit based on an algorithm that minimises ISI jitters. The algorithm selects the decision result at the optimal sampling-phase point based on an estimate of the neighbouring data pattern. The algorithm we use is rather simple and the final output of the current bit b_i is expressed as

$$
\begin{aligned}
b_i = (b'_{i+1,0}\bar{b}'_{i-1,0} + b'_{i+1,0}b'_{i-2,0})b'_{i,\Delta} + (\bar{b}'_{i+1,0}\bar{b}'_{i-1,0})b'_{i,0} \\
+ (\bar{b}'_{i+1,0}b'_{i-1,0} + b'_{i-1,0}\bar{b}'_{i-2,0})b'_{i,-\Delta}
\end{aligned} \tag{1}
$$

where $b'_{j,0}$ ($j = i-2,\ i-1,\ i+1,\ i+2$) is the preliminary decoded results of the neighbouring bits, their logic combination values in the parenthesis decide which sampled result of the current bit at different phase points ($b'_{i,-\Delta}$, $b'_{i,0}$ and $b'_{i,\Delta}$) gives the final output, respectively.

The results of the Boolean calculation correspond to, as illustrated in Fig. 1, the relationship between the data pattern and pulse jitter. For example, if the bits right before and after the current ($b'_{i-1,0}$ and $b'_{i+1,0}$) could be both zero, the position of the current bit would not shift and $b'_{i,0}$ is picked. In other cases, consider a possible sequence of (00∗10) with ∗ being the current bit. If it is a '1', it is likely to shift to the right, thus we get $b_i = b'_{i,\Delta}$, i.e. the right-shifted sampling position is adopted as it could increase the probability of correctly capturing a 'one' bit.
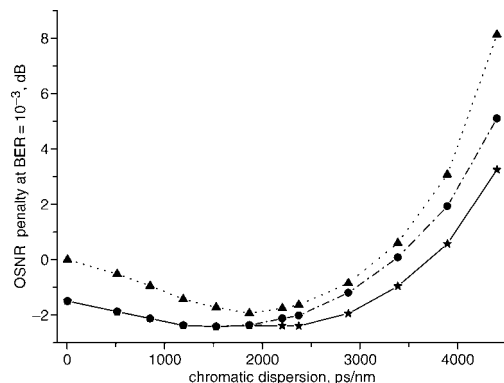

Fig. 3 *Simulated OSNR penalty for different receivers*

▲ Conventional ● QDS ★ SASO

The transmission under large residual CD is significantly improved by the SASO algorithm, as shown in Fig. 3. The three curves are obtained with the use of different receivers: a conventional one, a quasi-Dirac sampling (QDS) receiver [10], and the SASO receiver. The performance of the SASO receiver under large CD is further improved over the QDS case. At a residual dispersion of 4500 ps/nm, the OSNR penalty is reduced by another 2 dB on top of the 3 dB reduction via the QDS receiver. The BB performance can be further improved if the algorithm in [10] is employed instead of (1) when the CD is absent.

Conclusions: We propose for the first time, to the best of our knowledge, a novel detection technique that can compensate for dispersion-induced pulse distortion in duobinary systems through optimisation of the sampling phase by using the preliminary sequence information. We show that it could be implemented by combining an over-sampling receiver frontend, [7], and a simple digital processing unit. Its simplicity may render it attractive for high-speed, low-cost applications.

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