Wide Dynamic Range 10-Gb/s DPSK Packet Receiver Using Optical-Limiting Amplifiers

Yikai Su, *Member, IEEE*, Xiang Liu, *Member, IEEE*, and Juerg Leuthold, *Member, IEEE*

***Abstract*—We demonstrate a method to extend the dynamic range (DR) of 10-Gb/s differential phase-shift keying (DPSK) receivers in presence of burst-mode data. We achieve a DR of 25 dB by operating linear optical amplifiers in saturation and benefiting from fast optical-limiting amplification. A fixed decision threshold as enabled by DPSK receivers with balanced detection eliminates the need for guard times and removes inherent sensitivity penalty associated with the adaptive threshold as in conventional ON–OFF keying receivers.**

***Index Terms*—Dynamic response, optical receivers, packet switching, phase coding, semiconductor optical amplifiers (SOAs).**

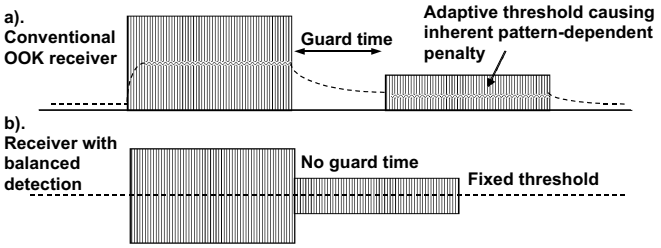

Fig. 1. Threshold in (a) conventional OOK receivers, and (b) balanced-detection receivers.

I. Introduction

BURST-MODE optical receivers are essential for packet-switched photonic networks. However, there have been challenging problems in burst-mode clock and data recovery [1]–[4]. Burst-mode data recovery suffers from the large power fluctuation between adjacent packets, which originates from the large variation of fiber-transmission and node-splitting losses in transport paths. The maximum power fluctuation that a burst-mode receiver can tolerate at a certain bit-error rate (BER) is defined as the dynamic range (DR) of the receiver input power. Inherently, conventional ON–OFF keying (OOK) receivers experience sensitivity penalty associated with the adaptive decision threshold in handling packets with largely varying amplitudes. In [4], such a penalty was analyzed and shown to be dependent on the decay time constant of the adaptive threshold τ_f, which is determined by the receiver DR in decibels and the minimum allowable guard time between adjacent packets t_g, $\tau_f = 4.343\ t_g/\mathrm{DR(dB)}$. The penalty increases with short time constant τ_f due to the fact that the threshold decays away from optimum decision level in the case of a string of "0s". In conventional OOK receivers, there is a fundamental conflict between the realization of short guard time with wide DR and good receiver sensitivity performance. Differential coding schemes employing balanced detection, such as Manchester coding [5] and differential phase-shift keying (DPSK) [6], provide an effective approach to eliminating the receiver sensitivity penalty associated with the varying decision threshold. In principle, balanced detection receivers can also remove the guard time between packets provided that the packets arrive in phase and the clock is always present, without inducing any receiver sensitivity penalty. Fig. 1 visualizes the difference of threshold settings in the two types of receivers. Note that the threshold in an OOK receiver varies depending on the data pattern, and the receiver would not work in the extreme case where there is no guard time between two adjacent packets. In contrast, a balanced detection receiver operates with a constant decision threshold, which does not incur pattern-dependent sensitivity penalty as seen in OOK receivers. Previously, a DPSK receiver with a fixed decision threshold to tolerate 10-dB power fluctuation with 3.2-ns guard time was successfully demonstrated [6]. In a balanced-detection packet receiver, the minimum input power requirement is determined by the sensitivity of the receiver, while the maximum power is limited by the linearity of the photodiodes as well as the their input-power damage threshold. The DR of the balanced receiver we used in the experiment is narrow since it is designed with low-resistance termination of the photodiodes followed by an electrical amplifier, rather than high trans-impedance receiver type that provides good sensitivity. To improve the receiver sensitivity, an erbium-doped fiber amplifier (EDFA) is employed as the optical preamplifier, which determines the sensitivity performance. We note that the DR of the optically amplified receiver cannot be increased by operating the EDFA in saturation regime. Even when the EDFA is saturated by the high-power packets, the low-power packets experience the same reduced gain due to the slow gain recovery time of the EDFA. To improve the DR of a packet receiver while maintaining the same receiver sensitivity, an optical-limiting amplifier following the EDFA is needed to provide a strong and fast gain saturation effect in order to equalize the packets with different input power levels over a very short period of time, preferably within a bit period.

In this letter, we demonstrate a method to extend the DR of 10-Gb/s DPSK packet receivers to 25 dB, and we show that such a receiver can operate under the extreme condition where no guard time is present, as shown in Fig. 1(b). The wide DR is

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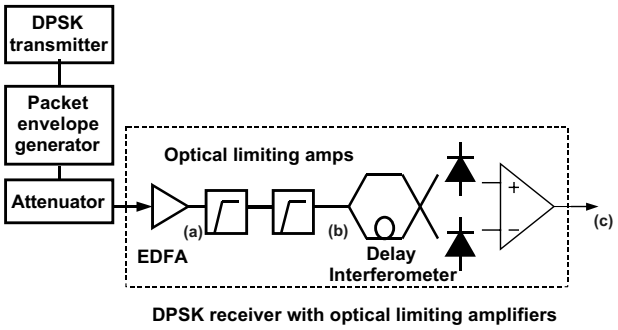

Fig. 2. Simplified schematic of the experimental setup.

achieved by using fast-saturating optical amplifiers. We focus on the DR performance of the data recovery with constant clock for in-phase packets without guard time. The investigation of burst-mode clock recovery is beyond the scope of this letter.

II. Experimental Setup

Standard semiconductor optical amplifiers (SOAs) could be used as limiting amplifiers due to their ability to provide high gain and a strong but fast saturation characteristic. However, the SOA gain roll-off might be a source of chirp, which would be particularly detrimental for the DPSK signals. Use of gain-clamped SOAs may remedy this effect for the DPSK signals. Yet turn-on oscillations that come along with laser cavities might occur for high input power signals that lead the gain-clamped SOA into saturation [7]. Recently, linear optical amplifiers (LOAs) have been introduced [8]. As LOAs employ short gain-clamped vertical cavities, we expect these oscillations to be shorter, and thus, allow operation at 10 Gb/s.

Fig. 2 shows the simplified experimental setup for the packet reception. The 10-Gb/s transmitter generates DPSK signals by driving a $LiNbO_3$ Mach–Zehnder (MZ) modulator biased at its null. The data of the DPSK transmitter is $2^{11}-1$ pseudorandom bit sequence (PRBS) signal. The packet envelope generator is based on an electroabsorption modulator (EAM) with a maximum extinction ratio of $\sim$30 dB. By applying square-wave signal on the EAM, in-phase packets with different levels can be generated. The envelope clock is synchronized with the bit pattern period, therefore, the bit-error-rate tester (BERT) can be gated in measurement time rather than through the use of RESYNC function. This enables measurement of small blocks as short as 2 ns to accurately investigate the receiver performance during the transition between two packets. The period of the frame clock from the pattern generator is 32 times of the PRBS sequence length, or 6.5536 μs. We use the frame clock as reference to generate alternating high–low packet envelopes each having 50% duty cycle of the 6.5536-μs period.

The wide DR receiver consists of an EDFA as a preamplifier, two cascaded LOAs as optical-limiting amplifiers, a delay interferometer with 100-ps relative delay between the two branches, balanced photodetectors, and an electrical amplifier. Two LOAs are used to obtain sufficient gain (each LOA has a small signal gain of only 11 dB) and better saturation characteristics. Further improvement in optical-limiting amplification is possible by employing LOAs with higher gain or by cascading more

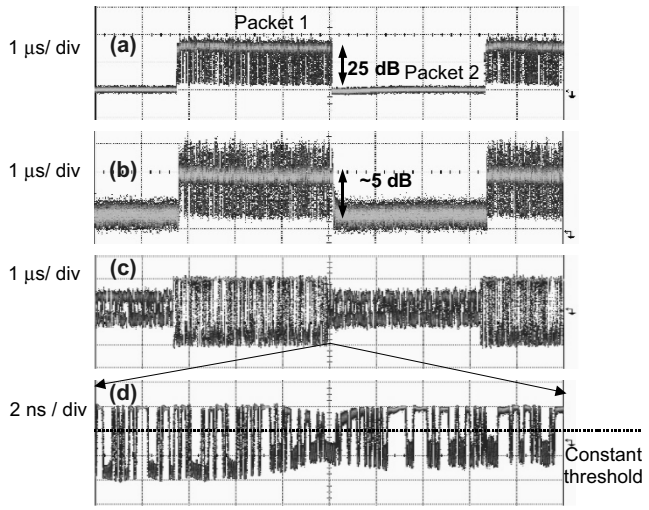

Fig. 3. (a) Optical DPSK signal after the preamplifier, (b) optical signal after the LOAs, (c) electric signal after balance detection and amplification, and (d) zoom-in picture of the electric signal.

LOAs. Each LOA is driven with $\sim$100 mA current. After the delay interferometer, the DPSK signal is demodulated and detected by the balanced detectors to generate electrical signal with $+/-$ amplitude. The measured electrical-receiver sensitivity defined at the input of the delay interferometer is 0 dBm. The delay interferometer exhibits $\sim$4-dB insertion loss. The maximum allowable optical power into the interferometer is $\sim$10 dBm to maintain the linearity of the photodiodes, therefore, the DR of the electrical receiver is $\sim$10 dB. In the BER measurement the BERT threshold is fixed close to zero.

III. Results

We create alternating high–low packets with 25-dB difference in amplitude by driving the EAM with a square-waveform signal having a period of 6.5536 μs and 50% duty cycle. Fig. 3 shows the waveforms of DPSK optical signal at the preamplifier output [Fig. 3(a)], optical signal equalized by the LOA [Fig. 3(b)], and the electrical amplifier output [Fig. 3(c)]. Fig. 3(d) is a zoom-in picture of the electric signal showing that all bits are recovered at the transition. The fact that threshold setting is not exactly at zero level can be attributed to the imperfect balance between the two photodiodes and the delay interferometer arms. Note the overshoot on top of the strong input power packets in Fig. 3(b), which can be attributed to the dynamic response of the LOAs associated with the bit transition of the DPSK data generated by the MZ modulator that is biased at null. The overshoot is then suppressed by the electrical limiting amplifier at the last stage.

We first measure the BER for all the packets by setting the BERT in continuous mode. The square line in Fig. 4 shows the BER versus the average received power, where the high input-power level packet is 3-dB higher than the average measured power, while the low input-power packet is 22 dB (3–25) lower than the average power. To investigate the limiting factor in the DR, we extrapolate a BER curve for the low input-power packets. The power of the low-level packets is 22 dB below the average measured power, the dashed line in Fig. 4 shows the extrapolated BER versus the power of the low-level packets,

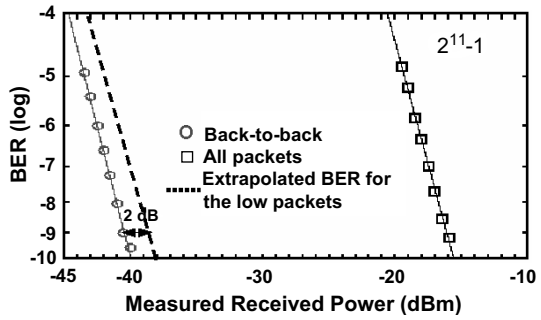

Fig. 4. BER measurement of back-to-back continuous data stream and packet reception with 25-dB DR. Dashed line is the derived BER curve for the low-level packet, showing 2-dB penalty compared to back-to-back continuous data measurement.

including the errors occurring from the transition of adjacent packets. Compared to the back-to-back sensitivity with continuous data stream, there is a 2-dB difference for the low input-power packets in switching mode. To investigate the errors occurred in low-power packets, high-power packets, and during the transition, we operate the BERT in the gating mode with a measurement time of 2 ns and scan over the whole period of 6.5536 μs. We find that the high-power packets are error-free. Low-power packets show similar performance as back-to-back without additional power penalty, while the transition between the two packets causes a higher error rate than the noise-limited low input-power packet. This can be attributed to the chirp added by the EAM when it is being switched, which distorts the phase coherence between adjacent bits in the transition time.

LOAs show good performance in suppressing high-power packet amplitude. As can be seen in Fig. 3, the 25-dB difference in amplitude between the two packets reduces to $\sim$5 dB after two LOAs. However, when the second LOA is replaced with a standard SOA, the receiver shows an error floor of 10^{-7} even after the operation conditions of all components are reoptimized, possibly due to the chirp and extinction ratio degradation induced by the saturating SOA [7].

The dynamic input power range of the receiver in the demonstration could be wider if stronger output power from the transmitter were available. In our setup, the maximum power of the continuous data stream injected into the EAM is 6 dBm, while the EAM and the attenuator have a minimum loss of 19 dB. The maximum power of the high-power packet is then -13 dBm. At this condition, we did not observe bit errors from the high-power packets, therefore, we expect that a wider DR would be achievable if an additional booster amplifier were placed after the DPSK transmitter and the EAM still has sufficient extinction ratio to generate packets with enough power difference. In addition, the DR of the receiver could be further increased if a balanced receiver with better sensitivity performance were available.

IV. Conclusion

We have demonstrated a method to extend the DR of 10-Gb/s DPSK packet receivers. For DPSK receivers with balanced detection, the optimal decision threshold is fixed regardless of the packet power, which enables zero guard time between packets. The wide DR of 25 dB is achieved using LOAs in the saturation regime as fast optical-limiting amplifiers that outperform standard SOAs.

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